Power Chips for Efficient Energy Conversion

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Abstract. The Power Chips technology employs a gap of 4-10 nanometers in a gap diode to allow for efficient thermal conversion with very low thermal leakage. The design ΔT is on the order of 400 degrees single stage, with operation possible from 1 K to 1600 K, depending on configuration and meeting engineering challenges. Efficiency is projected to be in the range of 70% of Carnot-defined maximum. R&D work on this approach has been in progress since 1997. The main technical challenge of fabricating and maintaining the required gap has been overcome; thin film and packaging issues remain. The technology is anticipated to be ideal in terms of size, weight, efficiency, and reliability. Power Chips can be packaged identically as conventional thermoelectrics making them a drop-in replacement in many cases including RTGs. Applications for Power Chips include RTGs as well as thermal conversion from a waste heat stream or solar-thermal conversion.

INTRODUCTION

Efficient solid-state thermal conversion has been much-sought after for space applications for decades. To date, work has focused on two primary directions: thermionic converters (Houston, 1959), which are capable of high power and efficiency only at temperatures in excess of 1700K, and thermoelectric converters, which operate at low temperatures but suffer from low efficiency. Neither of these approaches has made great strides since their early development days; thermionic converters reached a thermal efficiency of 23% over 30 years ago (Wilson, 1967), and thermoelectrics have failed to find the ideal high ZT material, though advanced layering techniques with existing materials appear to yield improved results. The workhorse materials of thermoelectrics, Bismuth Telluride, SiGe and the TAGS alloys have all been known and unimproved for several decades (Allen, 2003).

The need for a better power conversion technology is well established. RTGs are directly reliant on thermoelectric converters today, and their low efficiency means that the radiator and radioactive heat source have to be quite large. If the percentage of carnot efficiency could be improved from 5% to greater than 70%, it would have a stunning impact on the reduction of space and planetary probes. Power Chips could be an enabling technology for ion thrusters, giving them considerably more power than they presently enjoy. Additionally, solar-thermal conversion may be an option for such a conversion technology, potentially reducing the cost and complexity of solar arrays.

The objectives of this work are to design and build efficient solid-state thermal converters which enjoy the high efficiency and power of thermionic converters, but also are capable of generating power across a very wide range of temperatures. Power Chips in theory can function from 1 K to up to 2000 K (depending on lifetime requirements), with a ΔT across a single stage of hundreds of degrees. Such a solution would have a wide-ranging impact on space power systems.

DEVELOPING AN ENTIRELY NEW, HIGHLY EFFICIENT THERMAL CONVERSION TECHNOLOGY FOR A VERY WIDE RANGE OF APPLICATIONS

The Power Chip is a variant of the thermionic converter, but it is perhaps best understood as an upgraded thermoelectric device. Thermoelectrics suffer from low efficiency because heat transfer can move from one side of the device to the other using phonon transfer, instead of electron flow.

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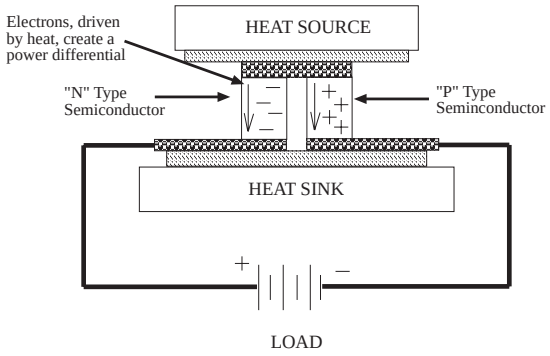


FIGURE 1. Typical Thermoelectric Power Conversion.

The solution to this problem has been sought in advanced materials, trying to find a material with a high electrical conductivity but low thermal conductivity. These "high ZT" materials have been elusive to date, though some recent advances have been made by employing heterostructures or using very advanced thin film layering (Venkatasubramanian, 2001; Hagelstein, 2002; Allen, 2003). Still, the core problem remains, that as long as there is an intermediate layer between the hot and cold side, the bulk of the heat flow will be transferred via phonon coupling and not electron flow, resulting in inefficiency.

The Power Chip addresses both the materials challenge of thermoelectrics and their low efficiency by employing a gap between the emitter and collector diodes.

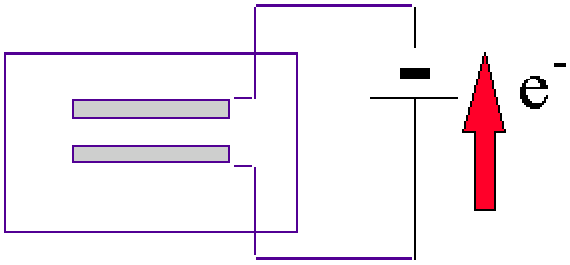


FIGURE 2. Gap-Diode Power Converter.

The ideal material is in fact the absence of material -- a vacuum is both electrically conductive and thermally insulating. With the gap, the Power Chip can formally have an infinite ZT, since the vacuum allows for electrons to tunnel from the hot side to the cold side, but bars phonon coupling on the reverse path. The calculated efficiency is on the order of 70% of the carnot-defined maximum possible for any given delta-t.

REQUIREMENTS

But in order for a Power Chip to function, the following requirements have to be met:

1. The gap must be relatively uniform
2. The local surface must have a roughness of < 3 nm to maximize emission and minimize contact across the gap.
3. The gap must be maintained in a variety of operating conditions, compensating for thermal expansion, vibration, and other forces.

4. Ideally, the gap should be variable, thus creating a filter which helps modulate the quantity and "quality" of the electrons moving across the gap. A large gap reduces output and maximizes efficiency, while a small gap increases output, but at reduced efficiency.

5. Thin films must be used so that the emitter and collector have a difference in work function, allowing for a voltage output when electrons cross the gap.

6. In order for the Power Chip to be useful in a power generation system, there needs to be an excellent thermal contact to the heat source and the heat sink.

7. Finally, electrical and thermal packaging must be designed and applied to the core Power Chip device in order to integrate the component into a system.

Power Chips development work to date has been addressing these requirements. The solutions sought, and their results to date are as follows:

Uniform Gap

The Power Chip is fabricated by using a surface replicating technique. A layer of silver is deposited or sputtered on a polished silicon substrate, followed by a layer of titanium, and capped with a thick layer of copper.

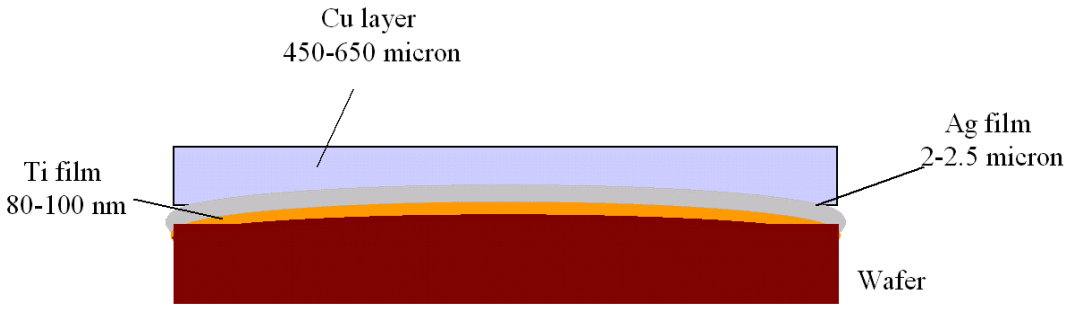


FIGURE 3. "Sandwich" Prior to Opening.

The adhesion between the silver and titanium is carefully limited. Because of the different thermal expansion coefficients of silicon and copper, applying tension and cooling the resulting "sandwich" breaks the two sides apart.

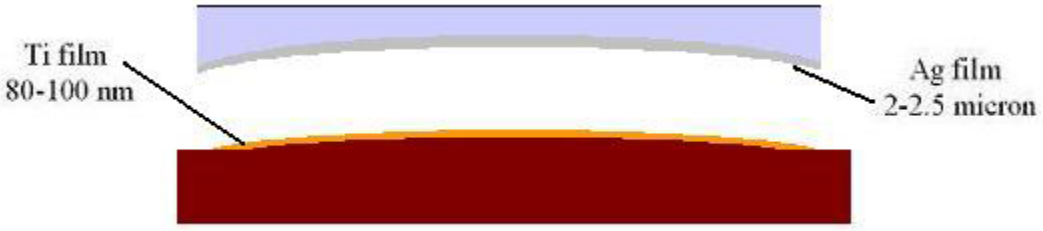
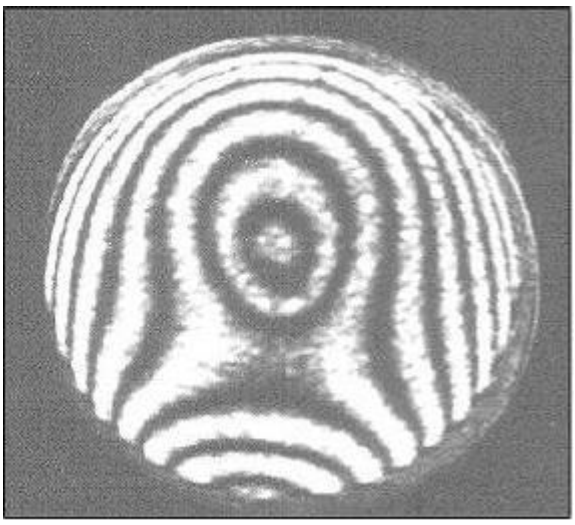


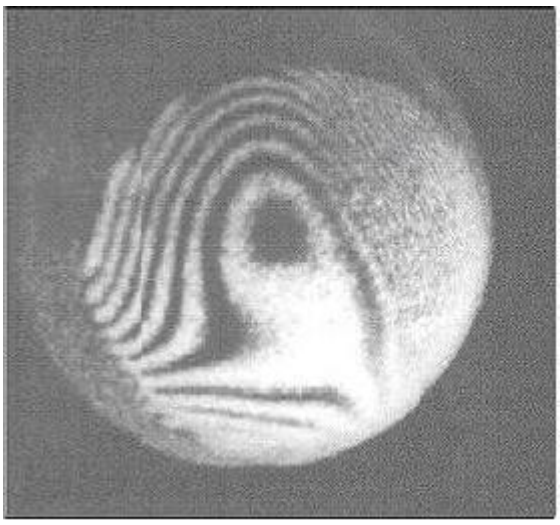
FIGURE 4. Sandwich When Opened.

Tests have shown that this break is clean - there is virtually no titanium on the silver, and no silver on the titanium. The two sides of the sandwich are brought back together, and the gap is created.

FIGURE 5. Sandwich in Operating Position. Gap is Created Using Mirrored Diodes.

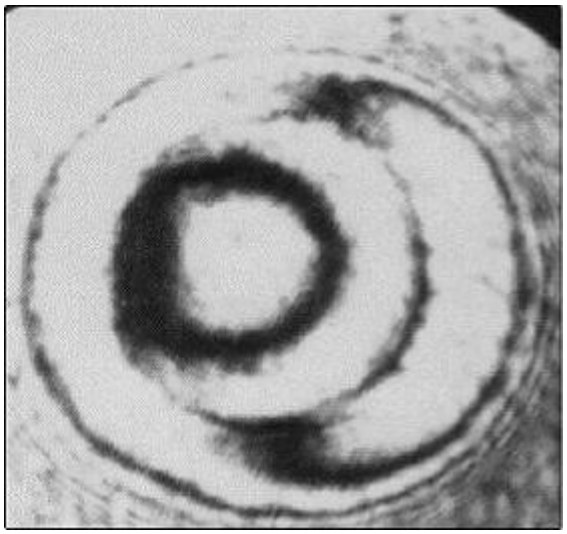


(a) Earlier Si/Ti Electrode.

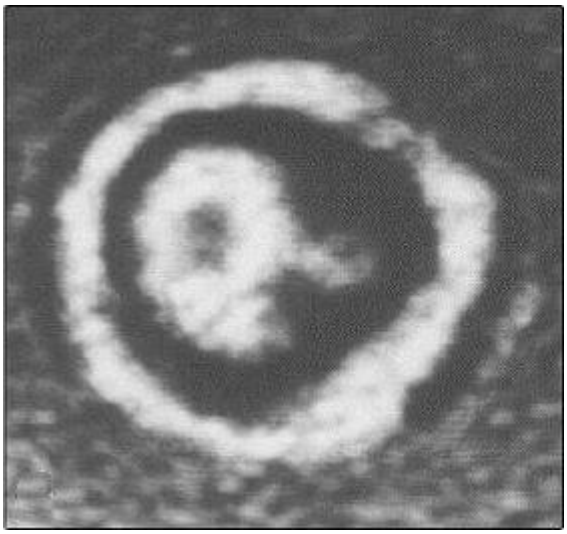


(b) Earlier CuAg Electrode.

FIGURE 6. Interferograms Showing the Curvature of An Electrode Pair From Earlier Development Efforts. Distance Between the Rings: 317 nm. Diameter: 28 mm.



(a) More Recent Si/Ti Electrode.



(b) More Recent CuAg Electrode.

FIGURE 7. Interferograms Showing The Curvature of a More Recently Produced Electrode Pair. Increased Flatness Is Demonstrated by Significant Reduction in Contour Lines.

Interferograms show that the surfaces mirror each other to the extent required to achieve this goal. To date, dozens of sandwiches have been created which meet this requirement, with a high yield.

Local Roughness

In order for tunneling emission to occur across the bulk of the emitter's surface, a surface which lacks large surface features and grains is required. If large grains are present, it would make the overall gap of < 10 nm impossible, and even if grains are "mirrored" on the other side of the sandwich, lateral (x axis) thermal expansion would short circuit the device. The problem was solved by using polished silicon wafers, and controlling the silver growth layer carefully to prevent granularization. Using a Zygo profilometer, it was shown that the surface of the collector-side of the sandwich is locally flat to < 1 nm.

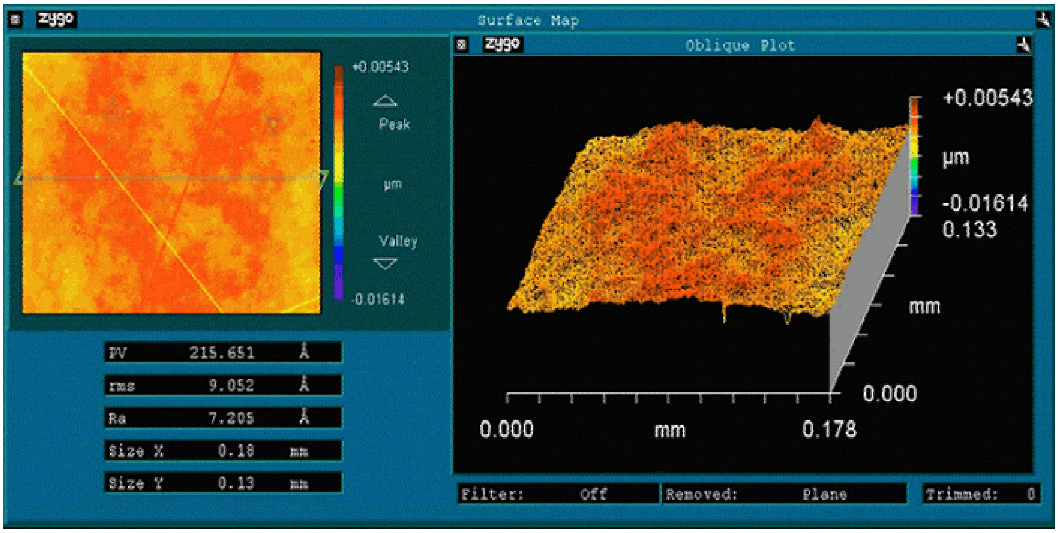


FIGURE 8. 3-D Plot of an 0.18mm X 0.13mm Area of a Cu/Ag Electrode.

Gap Maintenance

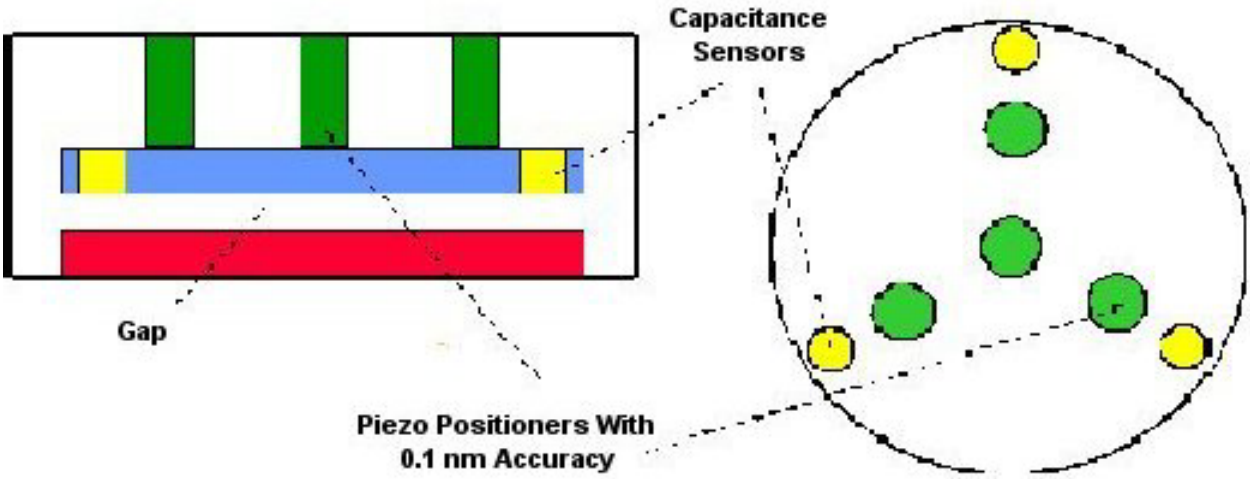
Expansion of the sandwich materials by a few nanometers, sufficient to close any created gap, can occur as a result of thermal expansion which would regularly occur in operation. Part of the solution is to match the bulk materials used for the emitter and collector, such that the collector (which operates at a colder temperature than the emitter), has a thermal expansion coefficient up to five times that of the bulk material on the emitter side. When fabricated at the right temperature, this solution allows the materials to stay generally matched for thermal expansion in the operating temperature region, and the danger to gap maintenance via lateral thermal expansion is minimized.

Additionally, however, it is necessary to compensate for direct (y axis) thermal expansion as well as externally-supplied vibration. For this reason piezo elements were chosen to provide gap regulation. The gap itself is measured indirectly using capacitance sensors. Because piezo elements react very quickly, this system allows for rapid correction to both thermal expansion and vibration, as well as any other forces which would alter the gap spacing outside of the desirable operating parameter. The ideal gap can be readily maintained in this manner. Fig. 9 shows four separate piezo units, able to independently compensate for changes in the gap.

Gap Variation

Because the Power Chip needs to be able to supply power, it is desirable to be able to trade off efficiency for output. The gap size is one way of controlling electron flow, and hence power output. Depending on the operating temperature and operating characteristics, the gap can be in the range of 2-10 nm, and sometimes it would be useful

to expand it beyond this size to turn off the bulk of the electrical output. The piezo positioners used for gap maintenance also are used to supply this specific control.



(a) Side View. **(b)** Plane View.

FIGURE 9. Inter Electrode Gap Regulation Using Piezo. Feedback Mechanism Uses Capacitors and Piezo Units.

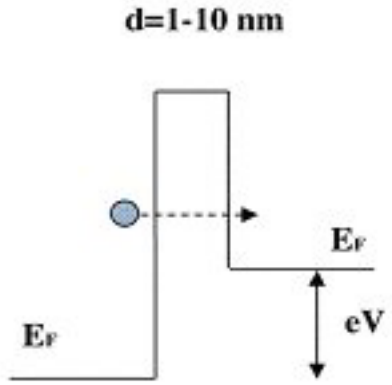


FIGURE 10. Thermo-Tunnel Converter 1 K – 2000 K: Potential Profile for a Power Chip. Electrons Tunnel Across Gap of Width d To a Region of Higher Potential, thus Generating a Voltage Output eV.

Thin Films

Simple tunneling current across a gap will not create useful power out, as shown by fig. 10. The output would be high current, at a voltage of zero. In order to create a voltage output, the diode materials must have a differential work function. That work function, given in electron-volts, shows the voltage output. Voltage, then, is fixed for a Power Chip by the materials used in the thin film layers.

The current project goal is to apply a thin film to the emitter which lowers its work function. The ideal work-function differential depends on the desired output, efficiency, and operating temperatures of a specific Power Chip. Development goals at present are to use thin films on both sides of the diode, creating a work function difference of the order of 0.5-1.0 eV.

Thermal Interface

As Power Chips moved from a research project, which showed that nanoscale gaps between large diodes could be made and maintained, toward making devices which can be implemented in a power generation system, it became clear that if the piezo elements were in the thermal pathway, then they would be considerably less effective.

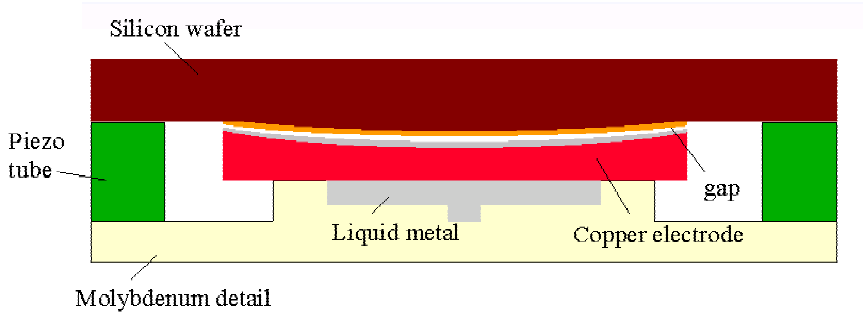


FIGURE 11. One Possible Production Configuration.

The latest design, shown in Fig. 9, has the piezo elements forming a circular ring around the core Power Chip device, allowing the thermal pathway to be comprised solely of bulk materials with good conductive properties. It is expected that feedback and other circuitry for gap maintenance will be located adjacent to the primary thermal pathway as well.

The interface shown in Fig. 9 is capable of withstanding an external pressure of approximately 100 p.s.i..

Electrical and Thermal Packaging

The Power Chip still needs to be packaged within a housing (including that shown in Fig. 9) which meets critical objectives:

1) Good thermal interface between Power Chips and the heat sink and heat source.

2) Optimized feedback electronics for gap maintenance and control

3) Good electrical interface with minimal ohmic resistance between the active power layers and the external power circuit. If the Power Chips are in an array (to allow for a higher output voltage), then the electrical interface needs to be optimized for this case.

4) Mechanical strength consistent with the shock and pressure environment for a given application.

The core challenge surrounding all of these objectives is that the hot and cold sides of the system are situated very close to each other – at the core of the Power Chip the distance is only a few nanometers, after all. Many power systems allow for truly macroscopic distances.

It is expected that the Power Chips development team has several key advantages when approaching the difficulty of the hot and cold sides being in close proximity. Primary among them include the fact that thermoelectrics technology has already tackled this problem and solved it satisfactorily. Solutions for use in space have already been developed for the radioisotope thermoelectric generators (RTG), which is a mature technology harnessing thermoelectrics. Thermoelectrics, like Power Chips, are high current, low voltage devices which are packaged in arrays. Both technologies rely on low contact potential and excellent thermal contacts across solid-state materials junctions. Power Chips can be fabricated so as to be very similar to thermoelectrics with regards to mechanical, thermal, and electrical interfaces – the only differences which would necessarily be externally apparent would be those which result from higher efficiency operation.

CURRENT PROJECT STATUS

Power Chips to date are still in the development phase. Sandwiches demonstrating the required gap have been fabricated and tested, showing gaps with the majority of the surface "active". Macroscopic heat pumping has been demonstrated for a related technology using the same sandwich technology (the Cool Chip). Work which still remains to be done before Power Chips can be used in space includes completing ambient-temperature devices with the required thin films, and then developing versions of the devices which are optimized for operation in the space environment. Power Chips plc is very likely to partner with other organizations in order to take the core Power Chips component and make it ready for space application. Depending on funding, high efficiency Power Chips devices could be ready for testing within one year.

KEY ADVANTAGES

Power Chips has the same advantages as thermoelectrics: solid-state (very low vibration) operation, a very high projected reliability, and no requirement for fluid loops to effect power production.

But in addition to the advantages inherent to thermoelectrics, Power Chips represents a number of critical advances, stemming from increased efficiency and superior performance. These advantages include:

- **Smaller mass of devices.** Power Chips are projected to have a specific heat flux of up to 40 watts/cm^2, and operate with a single-stage ΔT of up to 400°K. Consequently, the devices themselves are smaller even than a comparable thermoelectric stack.

- **Much smaller radiator needed.** If the efficiency is 25% then 75% of the input energy has to be discarded, requiring a large, heavy, and expensive heat sink. Power Chips, with a much higher projected efficiency, would make a much more competitive core power device for probes such as the Jupiter Icy Moons Orbiter, as well as other observatories and satellites (Morring, 2003).

- **Less heat fuel required.** A more efficient thermal converter would require far less radioactive mass than the 72 pounds of plutonium-238 required for the Cassini mission to Saturn (NASA, 1997).

CONCLUSIONS

The laboratory results to date show that the dominant technical challenge, that of creating and maintaining a small (5-10nm) gap across a macroscopic area, has been met. Engineering work remains before Power Chips can be tested for, and applied to, space applications.

When development is complete, Power Chips have considerable potential for power generation in space applications. The technology is essentially solid-state (the piezo units move only to compensate for thermal expansion and vibration, not to actively produce power), and has the potential to replace thermoelectrics as well as all other proposed and extant thermal-conversion technologies such as Stirling and Brayton cycles. There may also be a viable solar-thermal solution using solar concentrators, Power Chips, and a cold side heat sink.

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